AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A PLL circuit, comprising:

a variable-gain phase comparator outputting a signal proportional to a phase difference between a first input signal and a second input signal, and varying a phase difference gain;

a low-pass filter connected to an output terminal of the variable-gain phase comparator;

a plurality of VCOs connected to an output terminal of the low-pass filter;

a plurality of couplers connected one by one to an output terminal of the plurality of VCOs;

a frequency converter connected to each output terminal of the plurality of couplers, and converting a frequency of addition signal of the output signal from the plurality of couplers so as to output the second input signal; and

a control circuit controlling an on-off of operation of the plurality of VCOs.

2. (Original) The PLL circuit according to claim 1, wherein:

the frequency converter comprises a mixer circuit having two inputs; the addition signal of the output signal from the plurality of couplers is inputted to one of the two inputs; a local oscillator signal is inputted to the other of the two inputs; and

the frequency converter inputs an output of the mixer circuit to the variable-gain phase comparator.

3. (Original) The PLL circuit according to claim 1, wherein:

the frequency converter comprises a divider; the addition signal of the output signal from the plurality of couplers is inputted to the frequency converter; and the frequency converter inputs an output of the divider circuit to the variable-gain phase comparator.

4. (Original) The PLL circuit according to claim 1, wherein:

the variable-gain phase comparator is replaced with a phase comparator in which a phase difference conversion gain changes by the second signal amplitude, and a variable gain amplifier capable of varying a gain is interposed between the phase comparator and the frequency converter.

5. (Original) The PLL circuit according to claim 4, wherein:

the frequency converter comprises a mixer circuit having two inputs; the addition signal of the output signal from the plurality of couplers is inputted to one of the two inputs; a local oscillator signal is inputted to the other of the two inputs; and the frequency converter inputs an output of the mixer circuit to the phase comparator via the variable gain amplifier.

6. (Original) The PLL circuit according to claim 4, wherein:

the frequency converter comprises a divider; the addition signal of the output signal from the plurality of couplers is inputted to the frequency converter; and the frequency converter inputs an output of the divider circuit to the phase comparator via the variable gain amplifier.

7. (Original) The PLL circuit according to claim 1, wherein:

a plurality of low-pass filters connected in parallel is connected between the frequency converter and the variable-gain phase comparator, or is connected to the first input of the variable-gain phase comparator, and the PLL circuit further includes a control circuit for controlling an on-off of operation of the low-pass filters connected in parallel.

8. (Original) The PLL circuit according to claim 7, wherein:

the frequency converter comprises a mixer circuit having two inputs; the addition signal of the output signal from the plurality of couplers is inputted to one of the two inputs; a local oscillator signal is inputted to the other of the two inputs; and the frequency converter inputs an output of the mixer circuit to the variable-gain phase comparator.

9. (Original) The PLL circuit according to claim 7, wherein:

the frequency converter comprises a divider; the addition signal of the output signal from the plurality of couplers is inputted to the frequency converter; and the frequency converter an output of the divider circuit to the variable gain phase comparator.

10. – 14. (Cancelled)

15. (Previously Presented) The PLL circuit according to claim 2, wherein:

the variable—gain phase comparator comprises a Gilbert multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output current of the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

16. (Previously Presented) The PLL circuit according to claim 3, wherein;

the variable-gain phase comparator comprises a Gilbert multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output

current of the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

17. (Previously Presented) The PLL circuit according to claim 3, wherein:

the variable gain phase comparator comprises a Gilbert multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output current of the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

18. (Previously Presented) The PLL circuit according to claim 9, wherein:

the variable-gain phase comparator comprises a Gilbert multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output current of the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

19. (Previously Presented) The PLL circuit according to claim 15, wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output transistor, and

the PLL circuit inputs an output constant current of the reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

20. (Previously Presented) The PLL circuit according to claim 16, wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output transistor, and

the PLL circuit inputs an output constant current of the reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

21. (Previously Presented) The PLL circuit according to claim 17; wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output transistor, and

the PLL circuit inputs an output constant current of the reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

22. (Previously Presented) The PLL circuit according to claim 18, wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output transistor, and

the PLL circuit inputs an output constant current of the reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

23. (Previously Presented) The PLL circuit according claim 5, wherein:

the phase comparator is replaced with a phase comparator which is constructed in a manner that the variable current source of the variable-gain phase comparator described in claim 10 is replaced with a reference current generating circuit for generating a constant current output, and

an output signal amplitude from the variable-gain phase comparator inputted to the phase comparator is set smaller than k T/q.

24. (Previously Presented) The PLL circuit according claim 6, wherein:

the phase comparator is replaced with a phase comparator which is constructed in a manner that the variable current source of the variable-gain phase comparator described in claim 10 is replaced with a reference current generating circuit for generating a constant current output, and

an output signal amplitude from the variable-gain phase comparator inputted to the phase comparator is set smaller than Ic 'T/q.

25. (Currently Amended) A radio communication terminal apparatus, comprising:

a transmitter system including a quadrature modulator,

to which I and 0 signals are inputted, a PLL circuit connected to an output terminal of the quadrature modulator, and a power amplifier connected to an output terminal of the PLL circuit;

a receiver system outputting I and 0 signals; an antenna; and

an antenna switch interconnecting the antenna, the transmitter system and the receiver system,

the PLL circuit comprising the PLL circuit described in any of claims 1 to ~~19~~9 and 15 to 19.